## REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. Upon entry of this amendment, claims 1-26 will remain in the application, claims 27-46 having been canceled.

***Allowable Subject Matter***

Applicant would like to thank the Examiner for having agreed to a personal interview to discuss the patentable aspects of the invention. The interview was greatly appreciated.

***Allowable Subject Matter***

Referring to the most recent Office Action, the indication that claims 15, 16 and 18 would be allowable if rewritten in independent form is appreciatively noted. Applicant has rewritten the objected in allowed form thus reducing the issues under consideration.

***Restriction Election***

The originally presented claims 1-46 were subject to a restriction election. The claims of Group I (claims 1-26) were provisionally elected and examined by the PTO. Affirmation of this election by Applicant is hereby expressly provided.

As to non-elected claims 27-46, these claims have now been expressly canceled by Applicant, without prejudice, in order to reduce the issues under consideration. Applicant intends to pursue the subject matter of claims 27-46 in one or more separate divisional applications.

***Objection to Title***

The Examiner has objected to the title as not being descriptive. A new title has been presented which is believed to be more clearly indicative of the invention to which the claims are directed. Approval is requested.

***Specification Amendments***

Applicant has amended the specification to correct minor deficiencies. No new matter has been added. Approval is requested

***Art-based Grounds of Rejection***

The PTO has rejected elected Group I claims 1-14, 17, and 19-26 as being anticipated or otherwise unpatentable over the newly cited art. More specifically, claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by Fagan (GB 2,229,333A). Claims 3, 6, 11-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ruelke (US 6,459,889B1). Claim 2 was rejected under 35 U.S.C. 103(a) as being unpatentable over Fagen in view of Becker, et al. (US 5,612,975) and Webster et al. (US6,748,200). Claims 4-5, 13-14, 17, 19-22 were rejected under 35 U.S.C. 103(a) as being unpatenable over Ruelke in view of Dutkiewicz et al (US 5,629,960). Claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Sutterlin et al. (US 5,463,662). Claim 8 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Sutterlin, as applied to Claim 7 above, and further in view of Heck et al. (US 5,483,691). Claim 9 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Dutkiewicz, as applied to Claim 4 above, and further in view of Sutterlin – '662. Claim 10 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ruelke in view of Dutkiewicz, as applied to Claim 4 above, and further in view of Heck et al. '691. Claims 23-24, 26 was rejected under 35 U.S.C. 103(a) as being unpatentable over Fagan in view of Kotzian (US 5,014,013).

Applicant respectfully traverses the art grounds of rejection for the following reasons.

Applicant has amended its independent claims 1, 3, 11-13, 21-24 and 26 to more clearly indicate that the invention is directed to direct conversion receiver type architectures. The advantages of direct conversion receiver architectures (i.e., from RF direct to baseband conversion) as contrasted over heterodyne receiver architectures (i.e., from RF to an intermediate

frequency (IF) to baseband) are described in the specification. Most importantly, because there is no IF signal in the direct downconversion receiver, any gain normally provided by the IF amplifier in the heterodyne receiver would need to be provided instead at either RF or baseband in the direct downcoversion receiver. This poses serious design challenges particularly in the context of DC offset cancellation, variable gain amplification, and automatic gain control. The claimed invention is directed to a delicate balance of cooperating elements for maximizing a need in the art of direct conversion (downconversion) receivers capable of providing requisite signal gain and DC offset correction.

Independent claim 1, as amended herein, is directed to use of a gain controller coupled to measure an output from a digital VGA, and on the basis of this measurement to adjust both the analog as well as the digital VGA gains. This provides wide range gain adjustment in direct conversion receivers where no IF signal is available to facilitate gain adjustment in an intermediate step during downconversion. None of the cited references teach or suggest such an implementation.

Independent claims 3 and 11-13, as amended herein, are directed to an AGC loop in combination with a DC loop having multiple DC operating modes to provide variable gain during direct downconversion. Here again, none of the cited references show or suggest such a combination.

Independent claims 21 and 22, as amended herein, are directed to the aforementioned DC loop in accordance with an illustrative embodiment. The notion here of multiple operating modes in a DC loop operating in a direct conversion receiver architecture is neither taught nor suggested by the prior art. The operation and interoperability of a multi-loop DC loop operating in plural modes to facilitate DC offset correction during direct downconversion is believed to be patentably distinguishable over the cited prior art.

Remaining independent claims 23, 24 and 26 are directed to the conversion of a gain signal from logarithmic format to linear format so as to more readily perform digital multiplication of a desired downconverted signal with the gain signal. Since logarithmic formats

allow for a wide dB range distribution which is very important in direct conversion, a logarithmic to linear conversion addresses, among other issues, a unique gain stepping problem in direct conversion receivers. Here again, this is nowhere shown in any of the cited references.

In view of the above comments as well as the newly-presented amendments to the independent claims, reconsideration and withdrawal of the rejection to the claims now pending is earnestly requested.

The various dependent claims cited additional patentable features and should be allowable over the art of record for similar reasons as those given above in connection with the corresponding independent claims.

Accordingly, Applicant submits that all pending claims are allowable.

## CONCLUSION

In light of the amendments contained herein, Applicants submit that the application is in condition for allowance, for which early action is requested.

Please charge any fees or overpayments that may be due with this response to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: 3/28/05

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## CLEAN VERSION OF TITLE, SPECIFICATION AND CLAIMS

### IN THE TITLE

Please amend the title as follows:

-- *VARIABLE GAIN SELECTION IN DIRECT CONVERSION RECEIVER* --

### IN THE SPECIFICATION

Please amend paragraph [0010] as follows:

**[0010]** In another aspect, the operating mode of the AGC loop is selected based in part on the operating mode of the DC loop. Since these two loops operate (directly or indirectly) on the same signal components, they interact with one another. Techniques are provided herein for a loop to signal an event that may impact the performance of the other loop, so that the other loop can appropriately handle the event to minimize performance degradation. For example, if the DC loop is operated in an acquisition mode to quickly remove large DC offsets, large DC spikes can be produced that may have various deleterious effects on the AGC loop, then this event is triggered and the AGC loop may then be operated in a low gain mode or frozen altogether to minimize the effects of the DC spikes on the operation of the AGC loop.

Please amend paragraph [1039] as follows:

**[1039]** DC loop control unit 234a receives the I and Q outputs from summer 232a, determines the DC offsets in these outputs, and provides the coarse DC control to analog circuitry 222 within direct downconverter 120a. DC loop control unit 234b similarly receives the I and Q outputs from summer 232b, determines the DC offsets in these outputs, and provides the DC offset values of DC4I and DC4Q to summer 232b. Each DC loop control unit 234 is implemented with a gain element 236 coupled to an accumulator 238. Gain element 236 multiplies the input I or Q sample with a particular gain (DC gain 1 for unit 234a and DC gain 2 for unit 234b) selected for

that loop. Accumulator 238 then accumulates the scaled I or Q sample to provide the DC offset control for that loop.

Please amend paragraph [1042] as follows:

**[1042]** An implementation of the DC offset correction for a direct downconversion receiver, such as the one shown in FIG. 1, is described in further detail in U.S. Patent Application Serial No. 10/139,205, entitled "Direct Current Offset Cancellation for Mobile Station Modems Using Direct Downconversion," filed May 2, 2002, which is incorporated herein by reference.

## IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An automatic gain control (AGC) apparatus operable during direct conversion of RF signals comprising:

an analog variable gain amplifier;

a digital variable gain amplifier coupled to an output of the analog variable gain amplifier; and

a gain controller adapted to measure a signal output from the digital variable gain amplifier and to control the gains of the analog and digital variable gain amplifiers.

2. (Original) The apparatus of claim 1, further comprising:

a DC offset canceller interposed between the output of the analog variable gain amplifier and an input of the digital variable gain amplifier, wherein an AGC loop gain is varied according to an operating mode of the DC offset canceller.

3. (Currently Amended) A method of operating an automatic gain control (AGC) loop in combination with a DC loop during direct conversion of RF signals, comprising:

selecting a particular DC operating mode for the DC loop from among a plurality of possible DC operating modes;

operating the DC loop in the selected DC operating mode to correct for DC offset in a desired signal;

selecting a particular AGC operating mode for the AGC loop from among a plurality of possible AGC operating modes based on the selected DC operating mode; and

operating the AGC loop in the selected AGC operating mode to provide variable gain for the desired signal.

4. (Original) The method of claim 3, wherein the plurality of possible DC operating modes include an acquisition mode and a tracking mode.

5. (Original) The method of claim 4, wherein the acquisition mode has a wider loop bandwidth than that of the tracking mode and is used to more quickly remove a large DC offset in the desired signal.

6. (Original) The method of claim 3, wherein each of the plurality of possible AGC operating modes is associated with a respective AGC loop gain.

7. (Original) The method of claim 3, wherein the plurality of possible AGC operating modes includes a normal mode and a low gain mode.

8. (Original) The method of claim 7, wherein the plurality of possible AGC operating modes further include a freeze mode.

9. (Original) The method of claim 4, wherein the selected AGC operating mode is a low gain mode when the selected DC operating mode is the acquisition mode.

10. (Original) The method of claim 4, wherein the selected AGC operating mode is a freeze mode when the selected DC operating mode is the acquisition mode.

11. (Currently Amended) A direct conversion receiver unit in a wireless communication system, comprising:

a DC loop configurable to operate in one of a plurality of possible DC operating modes to correct for DC offset in a desired signal; and

an automatic gain control (AGC) loop configurable to operate in one of a plurality of possible AGC operating modes to provide variable gain for the desired signal, wherein the particular AGC operating mode to be used is determined based on the particular DC operating mode selected for use for the DC loop.

12. (Currently Amended) A control apparatus adapted for use in a direct conversion receiver, comprising:

means for selecting a particular DC operating mode for a DC loop from among a plurality of possible DC operating modes;

means for operating the DC loop in the selected DC operating mode to correct for DC offset in a desired signal;

means for selecting a particular AGC operating mode for an automatic gain control (AGC) loop from among a plurality of possible AGC operating modes based on the selected DC operating mode; and

means for operating the AGC loop in the selected AGC operating mode to provide variable gain for the desired signal.

13. (Currently Amended) A method of operating a DC loop in a direct conversion receiver unit, comprising:

selecting a particular operating mode for the DC loop from among a plurality of possible operating modes that include an acquisition mode; and

if the selected operating mode is the acquisition mode,

operating the DC loop in the acquisition mode for a particular time duration to correct for DC offset in a desired signal, wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode, and

transitioning out of the acquisition mode after the particular time duration.

14. (Original) The method of claim 13, wherein the acquisition mode is selected in response to an event expected to result in a large DC offset in the desired signal.

15. (Currently Amended) A method of operating a DC loop in a receiver unit, comprising:

selecting a particular operating mode for the DC loop from among a plurality of possible operating modes that include an acquisition mode; and

if the selected operating mode is the acquisition mode,

operating the DC loop in the acquisition mode for a particular time duration to correct for DC offset in a desired signal, wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode, and

transitioning out of the acquisition mode after the particular time duration,

the acquisition mode being selected in response to an event expected to result in a large DC offset in the desired signal, where the event corresponds to a switch to new analog circuit stages to process the desired signal.

16. (Currently Amended) A method of operating a DC loop in a receiver unit, comprising:

selecting a particular operating mode for the DC loop from among a plurality of possible operating modes that include an acquisition mode; and

if the selected operating mode is the acquisition mode,

operating the DC loop in the acquisition mode for a particular time duration to correct for DC offset in a desired signal, wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode, and

transitioning out of the acquisition mode after the particular time duration,

the acquisition mode being selected in response to an event expected to result in a large DC offset in the desired signal, ~~The method of claim 14,~~ wherein the event corresponds to application of a new DC offset value to correct for static DC offset in the desired signal.

17. (Original) The method of claim 13, wherein the plurality of possible operating modes further include a tracking mode.

18. (Currently Amended) A method of operating a DC loop in a receiver unit, comprising:

selecting a particular operating mode for the DC loop from among a plurality of possible operating modes including at least an acquisition mode and a tracking mode; and

if the selected operating mode is the acquisition mode,

operating the DC loop in the acquisition mode for a particular time duration to correct for DC offset in a desired signal, wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode, and

transitioning out of the acquisition mode after the particular time duration, the transition being made from the acquisition mode to the tracking mode after the particular time duration.

19. (Original) The method of claim 13, wherein the particular time duration is further selected based on an expected amplitude of the DC offset in the desired signal.

20. (Original) The method of claim 13, wherein the particular time duration is further selected to minimize a combination of DC offset introduced in the desired signal and loop noise from the DC loop.

21. (Currently Amended) A DC loop for use in a direct conversion receiver unit, comprising:

a summer operative to subtract a DC offset value from a desired signal to provide a DC offset corrected signal; and

a loop control unit configurable to operate in one of a plurality of possible operating modes to provide the DC offset value, wherein the plurality of possible operating modes include an acquisition mode having a particular loop bandwidth, and wherein the loop control unit is operated in the acquisition mode, when selected, for a particular time duration inversely proportional to the loop bandwidth for the acquisition mode and to transition out of the acquisition mode after the particular time duration.

22. (Currently Amended) A direct conversion receiver unit, comprising:

means for selecting a particular operating mode for a DC loop from among a plurality of possible operating modes that include an acquisition mode; and

means for operating the DC loop in the acquisition mode for a particular time duration, if the selected operating mode is the acquisition mode, to correct for DC offset in a desired signal, wherein the particular time duration is inversely proportional to a loop bandwidth for the DC loop for the acquisition mode, and

means for transitioning out of the acquisition mode after the particular time duration.

23. (Currently Amended) In a direct conversion receiver, a method of digitally amplifying a desired signal, comprising:

receiving a gain represented in a logarithm format;

determining a difference between the received gain and a gain offset;

converting the difference, represented in the logarithm format, to an output gain represented in a linear format; and

digitally multiplying the desired signal with the output gain.

24. (Currently Amended) A digital variable gain amplifier (DVGA) for use in a direct conversion receiver comprising:

a first unit operative to receive a gain represented in a logarithm format and to determine a difference between the received gain and a gain offset;

a second unit operative to convert the difference, represented in the logarithm format, to an output gain represented in a linear format; and

a digital multiplier operative to multiply input samples with the output gain to provide output data.

25. (Original) The DVGA of claim 24, further comprising:

a multiplexer operative to multiplex inphase and quadrature input samples into a single sequence of samples, and wherein the digital multiplier is operative to multiply the inphase and quadrature input samples in a time-division multiplexed manner.

26. (Currently Amended) An apparatus for use in a direct conversion receiver for digitally amplifying a desired signal, comprising:

means for receiving a gain represented in a logarithm format;

means for determining a difference between the received gain and a gain offset;

means for converting the difference, represented in the logarithm format, to an output gain represented in a linear format; and

means for digitally multiplying the desired signal with the output gain.

**Claims 27-46. (Canceled)**

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